24. (New) The apparatus of claim 23 wherein said memory service interruption is a DRAM refresh operation.

25. (New) The apparatus of claim 23 wherein said memory service interruption is a memory maintenance operation.

26. (New) The apparatus of claim 23 wherein said first mode has an associated first burst size and said second mode has an associated second burst size.

27. (New) The apparatus of claim 23 wherein said memory buffer is a video buffer to buffer a video stream retrieved from memory.

28. (New) An apparatus comprising:

a video stream buffer;

a memory controller to occasionally perform an operation causing a memory service interruption; and

control logic coupled to said video stream buffer to maintain a first level of buffering in a first mode and to maintain a higher level of buffering prior to said memory controller performing said operation causing said memory service interruption.

29. (New) The apparatus of claim 28 wherein said operation is a DRAM refresh operation.

30. (New) The apparatus of claim 29 further comprising a processor, wherein said processor, said video stream buffer, said memory controller, and said control logic are all integrated into a single integrated circuit.